REMARKS

The Examiner objected to the drawings, alleging that "reference numbers 8, 10 in Fig. 2, reference number 26 in Fig. 4 are all associated with an empty "black box" which should have a corresponding label". In response, Applicants have amended the drawings.

The Examiner objected to the disclosure, alleging: "a/ on page 6, lines 6-7, and 11 (counted by hand), it is not clear "5 Î©, 10 Î©, 20 Î©, or 35 Î©", "1 k Î©", and "10 k Î©" represent. b/ on page 9, line 30 (counted by hand), it is not clear ".5 Î¼s" represents. c/ on page 10, lines 2 and 3 (counted by hand), it is not clear ".1 Î¼s", ".3 Î¼s" represent." In response, Applicants have included herewith in Appendix A pages 6, 9, and 10 of the originally filed patent application, and said pages do not show what the Examiner alleges. Moreover, the pages 6, 9, and 10 in Appendix A have line numbers, so that it is not necessary for the Examiner to count lines.

The Examiner objected to claims 12 and 14, alleging: "a/ in claim 12, "the chip-to-package connectivity" (line 1), and "the package semiconductor device" (lines 3-4) should be -- a chip-to-package connectivity -- and -- the semiconductor device --, respectively. b/ in claim 14, "a common I/O" (line 4) should be -- the common I/O --." In response, Applicants have amended claims 12 and 14 to clarify the invention.

The Examiner rejected claims 12-13 and 18-19 under 35 U.S.C. §112, second paragraph.

The Examiner rejected claims 12-16 and 20 under 35 U.S.C. §102(e) as allegedly being anticipated by Saitoh (U.S.P. 6,397,361).

The Examiner rejected claim 17 under 35 U.S.C. §103(a) as allegedly being unpatentable over Saitoh (U.S.P. 6,397,361).

Applicants respectfully traverse the §112, §102 and §103 rejections with the following arguments.

35 U.S.C. §112

The Examiner rejected claims 12-13 under 35 U.S.C. §112, second paragraph, alleging: "In claim 12, the limitation "the I/O" (line 6) has not been recited previously; therefore this term is indefinite. For examination purposes, "the I/O" is interpreted as -- the I/O of the semiconductor device --." In response, Applicants have amended claim 12 to clarify the invention.

The Examiner rejected claims 18 -19 under 35 U.S.C. §112, second paragraph, alleging: "In claim 18, the limitation "a fixture impedance coupled between the test fixture and at least one of the semiconductor device and a potential relative to the semiconductor device" is vague. The connection between "a fixture impedance" and "the test fixture", "at least one of the semiconductor device", "a potential relative to the, semiconductor device" is unclear. Furthermore, since only one semiconductor device has been recited in the claim (i.e., claim 14), therefore it is not clear why claim 18 recited "at least one of the semiconductor device"." In response, Applicants have amended claim 18 to clarify the invention.

35 U.S.C. §102

The Examiner rejected claims 12-16 and 20 under 35 U.S.C. §102(e) as allegedly being anticipated by Saitoh (U.S.P. 6,397,361).

As to claim 12, the Examiner alleges: "Saitoh discloses, in Fig. 7, a method of reduced pin count testing a chip-to-package connectivity of a semiconductor device (202), the method comprising: launching a transition signal (I) from a common I/O driver (720) on the semiconductor device (202); observing a response of the transition signal (1) at a point (718) within the semiconductor device (202); determining whether a chip-to-package connection (i.e., connection between point 718 and chip pad 110) associated with the I/O (110) of the semiconductor device (202) is faulty from the response of the transition signal (I)".

Applicants respectfully contend that Saitoh does not anticipate claim 12, because Saitoh does not teach each and every feature of claim 12. For example, Saitoh does not teach "providing an I/O driver and an I/O receiver on the semiconductor device, wherein a common I/O of the semiconductor device is electrically coupled to the driver and to the receiver, and wherein the common I/O is electrically interposed between the driver and the receiver". Applicants respectfully contend that FIG. 7 of Saitoh does not disclose an I/O receiver.

Based on the preceding arguments, Applicants respectfully maintain that Saitoh does not anticipate claim 12, and that claim 12 is in condition for allowance. Since claim 13 depends from claim 12, Applicants contend that claim 13 is likewise in condition for allowance.

As to claim 14, the Examiner alleges: "Saitoh discloses, in Fig. 7, an apparatus configured to launch a test signal (1) to a common I/O (110) of a semiconductor device (202)

from a driver (720) on the semiconductor device (202) which is associated with the common I/O (110) using reduced pin count testing, the apparatus comprising: a test fixture (702) configured to couple to the common I/O (110) of the semiconductor device (202); a weak driver impedance (712) coupled between the driver (720) and the test fixture (702); wherein the apparatus is configured to launch the test signal (I) through the weak driver impedance (712) and the common I/0 (110) to the test fixture (702) and evaluate with the common I/O (110) is faulty. As to claim 15, Saitoh disclose in column 12, lines 35-37, the weak driver impedance (712) includes a switchable impedance (i.e., adjustment resistor."

Applicants respectfully contend that Saitoh does not anticipate claim 14, because Saitoh does not teach each and every feature of claim 14. For example, Saitoh does not teach "an I/O receiver on the semiconductor device, wherein the common I/O is electrically coupled to the driver and to the receiver, and wherein the common I/O is electrically interposed between the driver and the receiver". Applicants respectfully contend that FIG. 7 of Saitoh does not disclose an I/O receiver.

Based on the preceding arguments, Applicants respectfully maintain that Saitoh does not anticipate claim 14, and that claim 14 is in condition for allowance. Since claims 15-16 and 20 depends from claim 14, Applicants contend that claims 15-16 and 20 are likewise in condition for allowance.

Applicants further contend that the rejection of claim 16 is improper, because Saitoh does not teach "wherein the weak driver impedance is an impedance having a resistive value of 1 KΩ or more." The Examiner alleges: "As to claim 16, Saitoh disclose in column 12, lines 35-37, the weak driver impedance (712) is an impedance having a resistive value of 1 KΩ." In response,

Applicants respectfully disagree because Col. 12, lines 35-37 of Saitoh discloses: "adjustment resistor 712 (typically **less than** 1 kO and preferably 0 O)" (emphasis added). Since "less than 1 KΩ" is outside the range of "1 KΩ or more", Applicants maintain that Saitoh does not anticipate claim 16 and is in condition for allowance.

35 U.S.C. §103

The Examiner rejected claim 17 under 35 U.S.C. §103(a) as allegedly being unpatentable over Saitoh (U.S.P. 6,397,361).

Since claims 17 depend from claim 14, which Applicants have argued *supra* to be patentable under 35 U.S.C. §102, Applicants maintain that claim 17 is not unpatentable under 35 U.S.C. §103(a).

In addition, Applicants contend that Saitoh does not teach or suggest the following feature of claim 17: "wherein the weak driver impedance is approximately 10 KΩ or more". The Examiner argues: "Saitoh discloses all limitations recited in the claim except for the weak driver impedance (712) is approximately 10 KΩ or more. It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the adjustment weak impedance (712) of Saitoh in the range of 10 KΩ or more, since it has been held that discovering an optimum value of a result effective variable involves only routine skill in the art. *In re Boesch,* 617 F.2d 272, 205 USPQ 215 (CCPA 1980)." In response, Applicants contend that the preceding argument by the Examiner has no relevance to claim 17.

CONCLUSION

Based on the preceding arguments, Applicants respectfully believe that all pending claims and the entire application meet the acceptance criteria for allowance and therefore request favorable action. If the Examiner believes that anything further would be helpful to place the application in better condition for allowance, Applicants invites the Examiner to contact Applicants' representative at the telephone number listed below.

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Coombs *et al.* Group Art Unit: 2829

Filed: 08/22/2001 Examiner: Tang, Minh Nhut

Serial No.: 09/682,345

Title: **METHOD AND APPARATUS FOR REDUCED PIN COUNT PACKAGE CONNECTION VERIFICATION**

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

APPENDIX A

Pages 6, 9, and 10 of Originally Filed Patent Application

C_F coupled in parallel with a device capacitance C_D and a package capacitance C_P. In practice, there are also resistances caused by the connections between the various elements of the system. However, for the purposes of the model shown in FIG. 2, the resistance caused by those connections are negligible compared to the other resistances discussed hereafter.

FIG. 2 includes two exemplary models 2 and 4 of a packaged semiconductor device 6 in a tester fixture. Using the AC CIO wrap method disclosed in U.S. Patent 6,058,496 to Gillis et al., previously incorporated herein by reference, a plurality of common inputs/outputs (I/Os) of a semiconductor device may be accessed and tested through control pads 8. Control pads 8 of the present invention may be configured as pins, pads, balls or any other electrical connections to the semiconductor device 6. Semiconductor circuitry 5 and 7, such as clock trees, latches, receivers, and the like, necessary for the AC CIO wrap method of Gillis, is coupled to the control pads 8. Box 10 represents a completed chip-to-package connection; box 12 represents a faulty chip-to-package connection. As shown in the modeled embodiment of FIG. 2, the packaged semiconductor device 6 is tested using weak drivers 9 and 15. As used herein, "weak driver" is intended to mean and include a driver which is configured to be sensitive to capacitive loading. For example, a conventional device driver is configured to be a 5 Ω, 10 Ω, 20 Ω or 35 Ω driver. By adding, for example, a large resistor (i.e. 1 kΩ or larger) in series with the driver to make it more sensitive to capacitive loading, the driver becomes a weak driver.

The weak driver of the embodiment modeled in FIG. 2 is a conventional driver, which has been modified by adding a 10 KΩ resistor R in series with the driver signal. A weak driver may also be formed using any method known in the art to increase the slope of a response to a transition at an input due to the impedance load coupled to it. One way to achieve this is to appropriately couple an additional impedance element, such as a resistor or a small field effect transistor (FET), between the driver elements and the

and speed response times. Temporarily placing a large resistor into series connection with a conventional driver for a portion of a test sequence allows the driver to be a weak driver for that portion of the test sequence. It should be made clear, however, that the switch is not required to practice the invention. Alternatively, a variable impedance may be used. Furthermore, although the embodiment of FIG. 4 shows the "Launch" and "Capture" paths from the tester to the I/O pad to be separate paths, it will be clear to one of ordinary skill in the art that the same launch bank, clock tree and control pad may be used for both the "Launch" and "Capture" paths.

In reference to FIGS. 4 and 5, a method of testing the chip-to-package connection of the I/Os of a semiconductor device using reduced pin count testing is disclosed. To begin, a testing sequence is begun (step 28), which may include performance of numerous I/O and other tests upon the semiconductor device. In step 30, a weak driver transition signal is then applied at a control pad to test a first I/O of a semiconductor device 22 coupled to a testing fixture 18. The timing of the initialization of the test signal transition is triggered into a launch latch L1 associated with a latch bank within the semiconductor device 22 (step 32). An observation latch L2 associated with the same or a different latch bank within the semiconductor device 22 is triggered when the transition signal, measured at a point 26 on the semiconductor device prior to the chip-to-package connection, reaches a predetermined threshold (step 34). Point 26 is only shown as one example of a location at which the transition signal may be measured. Other locations are also acceptable.

The predetermined threshold may be any threshold amount and may vary depending upon the test signal magnitude, the sensitivity of the testing and latch elements, and numerous other factors considered by those of ordinary skill in the art when determining an acceptable rise time for comparison. By a comparison of the timing and values captured in the first and second latches L1 and L2, a rise time or other transition value may be calculated which is indicative of whether the chip-to-package connection

for that particular I/O is faulty (step 36). The transition value from the latches may thereafter be converted to another value indicative of whether the chip-to-package connection is faulty if this is desirable in a particular application. One value conventionally useful to those of ordinary skill in the art in determining the slope of a transition signal is the resistive/capacitive (RC) constant of the system.

The transition value, such as the rise time, derived from the evaluation of the values stored in association with the launch and observation latches may then be compared to a connectivity threshold to determine if the transition value indicates a completed chip-to-package connection (step 38). For example, with a transition value equal to the rise time, a comparison may be made to an acceptable rise time threshold value to determine whether rise time is sufficiently slow to indicate an acceptable chip-to-package connection. This connectivity threshold may be selected from previous or subsequent tests of the same semiconductor device 22 to find an acceptable rise time compared to the other I/Os on the device, for example, or may be determined as a standard for all devices from previous tests on other devices of a similar kind.

By way of practical example, in reference to the graph shown in FIG. 3, if an acceptable rise value threshold of 80% were selected, the two lines would be clearly distinguishable. The first graph line 14, representative of the completed chip-to-package connection, does not rise to 80% of its maximum until around .5 μs. The second graph line 16, representative of a faulty chip-to-package connection, rises to 80% of its maximum before .1 μs. Therefore, any rise time threshold selected between these values, for example at .3 μs, may be acceptable for distinguishing between completed and faulty chip-to-package connections.

A similar procedure may be performed for each I/O chip-to-package connection for the semiconductor device from the same, or from any number of other control pads. For a particular I/O, a plurality of tests may be performed in conjunction with the